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PERSONAL AUTHOR(S): Wendell A. Henry

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FIELD	GROUP	SUB-GROUP	Pattern Recognition Image Processing

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

At the time of this report, the project has been authorized to spend $1,798,235.00 for the Phase 1, 2, and 3 tasks plus one optional task. The project has accumulated expenses of $1,085,804.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

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22a. NAME OF RESPONSIBLE INDIVIDUAL: Wendell Henry	22b. TELEPHONE (Include Area Code): (503) 690-1236 / 22c. OFFICE SYMBOL

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R & D Status Report

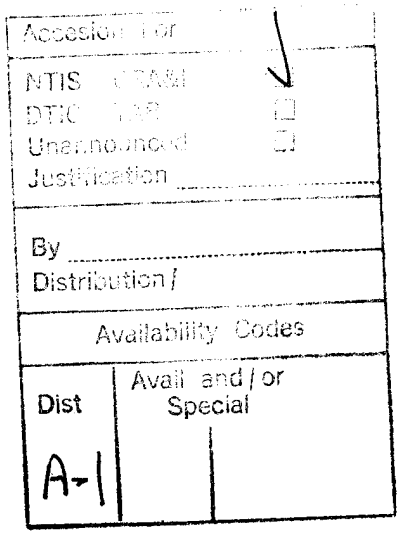
December 18, 1995

ARPA Order No.:

A407

Contractor:

Adaptive Solutions, Inc.
1400 NW Compton Drive, Suite 340
Beaverton, OR 97006



Contract No.:

N00014-93-C-0234

Contract Amount:

$1,997,949.00

Effective Date of Contract:

November 8, 1993

Expiration Date of Contract:

June 7, 1996

Principal Investigator:

Wendell A. Henry

Telephone Number:

(503) 690-1236

Title of Project:

High Performance Hardware and Software for Pattern Recognition and Image Processing

Title of Work:

R&D Status Report

Reporting Period:

September 1, 1995 through November 30, 1995

Disclaimer

Project Summary:

Phase 1 Objective:

Build PC/AT form-factor plug-in board using which implements the CNAPS architecture.

Phase 2 Objective:

Port CNAPS Software Development Kit to CNAPS PC board and Windows environment.

Phase 3 Objective:

Design and implement a C-callable function library providing image processing and neural network emulation operations which uses the CNAPS/PC board built in Phase 1.

Option 1 Objective:

Schematic design of portions of the next-generation CNAPS chip (X2).

Phase 1 summary:

Done.

Phase 2 Summary:

Done

Phase 3 Summary:

Work is in progress.

Option 1 Summary:

Work is in progress.

At the time of this report, the project has been authorized to spend $1,798,235.00 for the Phase 1, 2, and 3 tasks plus one optional task. The project has accumulated expenses of $1,085,804.00. Work on phases 1 and 2 are completed. Work on Phase 3 and the Optional task are in progress.

The contract stipulates that $1,997,949.00 is required for the completion of all tasks in Phases 1, 2, 3 and the exercised option. Therefore, an additional $199,714.00 of funding must be authorized to complete all phases of the project.

Description of Progress:

The previous Project R&D Status Report stated the following as the objectives for this reporting period:

1. *Support of the software and hardware products, including bug fixes, will continue.*
2. *Refinement of the Function Library architecture Specification will continue.*
3. *Implementation of C-callable library functions for Phase 3 will continue.*
4. *Verilog logic simulation for the X2 chip development will be completed.*
5. *Layout of the X2 will be completed.*
6. *DRC (Design Rule Checking) and LVS (Connectivity verification) of the X2 will be completed.*
7. *Analysis of X2 packaging options will be completed and a packaging decision made.*
8. *A C2 ASIC vendor will have been selected.*
9. *Layout floor planning for the C2 will be completed.*
10. *The Verilog RTL source code modifications for the C2 will be completed and validated.*
11. *Logical validation of the entire system, C2, X2, and board, will be completed.*

The following sections discuss the specific progress made in this reporting period in the hardware and software areas towards the stated objectives.

Hardware

Design:

No changes to the CNAPS/PC board hardware design took place this reporting period.

Two outside contractors were brought on board to accelerate the tape out of the X2, and additional internal resources were committed to the project. The design, layout, and verification progressed from 40% complete to 80% complete in the three month period. After a visit to the wafer foundry, a critical height requirement was determined which caused some relayout of the data path and resulted in 1 month delay in the tape out. Significant progress was made on the verilog logic simulation of the processor and sequencer, the work was not complete at the end of November. Two package design consultants were contacted and a contract with one was signed, a BGA package will be developed for the X2. The design delivery was 2 months behind schedule a the end of the period.

Testing:

Production shipments of the CNAPS/PC board continued.

Software

Design

We have continued to refine the C-Callable library specification. This includes coding guidelines for the various levels of software and Certification Testing to insure correct functionality. A final version of the specification will be created during the next report-

ing period. This certification will form the basis of the manual documentation which will accompany the library code upon completion of the project.

Implementation and Testing:

The library is organized into three basic groups of C-Callable functions:

1. Basic linear algebra
2. Image processing
3. Recognition

Coding and testing of the basic linear algebra functions is nearly complete, with 144 functions having been coded and tested for inclusion in the library. These functions have been coded according to the library specification, validating its integrity and exposing a few areas needing further refinement.

Deliverables

Delivery of ten (10) copies of the BP.DLL (Backpropagation Neural Network application software library) was delayed. It is expected that delivery will occur during the month of October, 1995. They will be delivered to:

PRC, Inc.	Attn.: Kevin Kitka	7 Units
Defense Group, Inc.	Attn.: Morgan Grover	1 Unit
David Taylor Model Basis	Attn.: David Hess	1 Unit
Army Research Lab	Attn.: Jeff DeHart	1 Unit

Issues and/or Concerns

None.

Plans For Next Reporting Period:

During the next three months work will continue on Phase 3 of the contract and the newly exercised contract option. The following are expected to be achieved:

1. Complete the library specification.
2. Begin generation of the library manual.
3. Complete the implementation and testing of the basic linear algebra portion of the library.
4. Begin the implementation of the image processing and recognition portions of the library.
5. Complete Verilog simulation of the X2.
6. Complete LVS and DRC of the design.
7. Complete tape out of the chip.
8. Complete the chip package design.

Fiscal Status:

Amount currently provided on contract:	$1,997,949.00
Expenditures and commitments to date:	1,085,804.00
Funds required to complete work:	$912,145.00

Authorized Phase funding:	$1,798,235.00
Expenditures and commitments to date:	1,085,804.00
Authorized Phase funds remaining:	$712,431.00

At the time of this report, the project has expenditures and commitments totaling 60% of the funds currently allocated for the contract.

Wendell A. Henry

Dec. 18, 1995
Date